

# Analog IC Design Homework 5 (1/6)

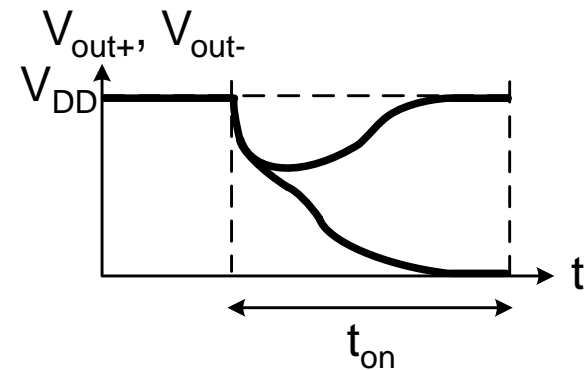
## ● 題目: Comparator with offset cancellation

1. 可使用 0.18 $\mu\text{m}$ , 16nm 或其他更先進製程 SPICE Model
2. Please optimize the Comparator shown in P.2 by calculation with  $\Delta V_{in} = -0.5\text{mV}$ 
  - ◆ Circuit operation is shown in P.2, the specifications are as follows:
    - Power supply  $V_{DD} = 1.8\text{V}$  (16nm ADFP  $V_{DD} \leq 1.05\text{V}$ )
    - Total compare time ( $T_c$ )  $\leq 1\text{ns}$ 
      - $T_c$ : Period between preamplifier get started and the output voltage of latch either is more than 1.7V or less than 0.1V
    - Load of Latch ( $C_L$ ) = 10 fF (Load is included in testbench file.)
3. Please use HSPICE to verify the comparator with  $t_{on} = 100\text{ns}$ 
  - ◆ Please use the attached testbench to test your circuit
4. Please design the **offset cancellation circuit** to cancel input offset voltage. Please use the size you have designed in 2., and **increase/decrease the width of positive/negative input by 0.1  $\mu\text{m}$** . You can design the circuit by yourself or refer to circuit in P.3
5. Please use HSPICE to verify comparator with offset cancellation
6. Compare and analyze the results between calculation and HSPICE verification

## ● Note

- ◆ Follow design rules of maximum and minimum transistor width and length
- ◆ For 4., you can use ideal switch(turn on:1m $\Omega$ , turn off:100M $\Omega$ ) and the external clk source to achieve offset cancellation circuit
- ◆ All transistor's body should connect to VDD or GND
- ◆ Please use Cadence Virtuoso to build schematic and export the .cir file for verification

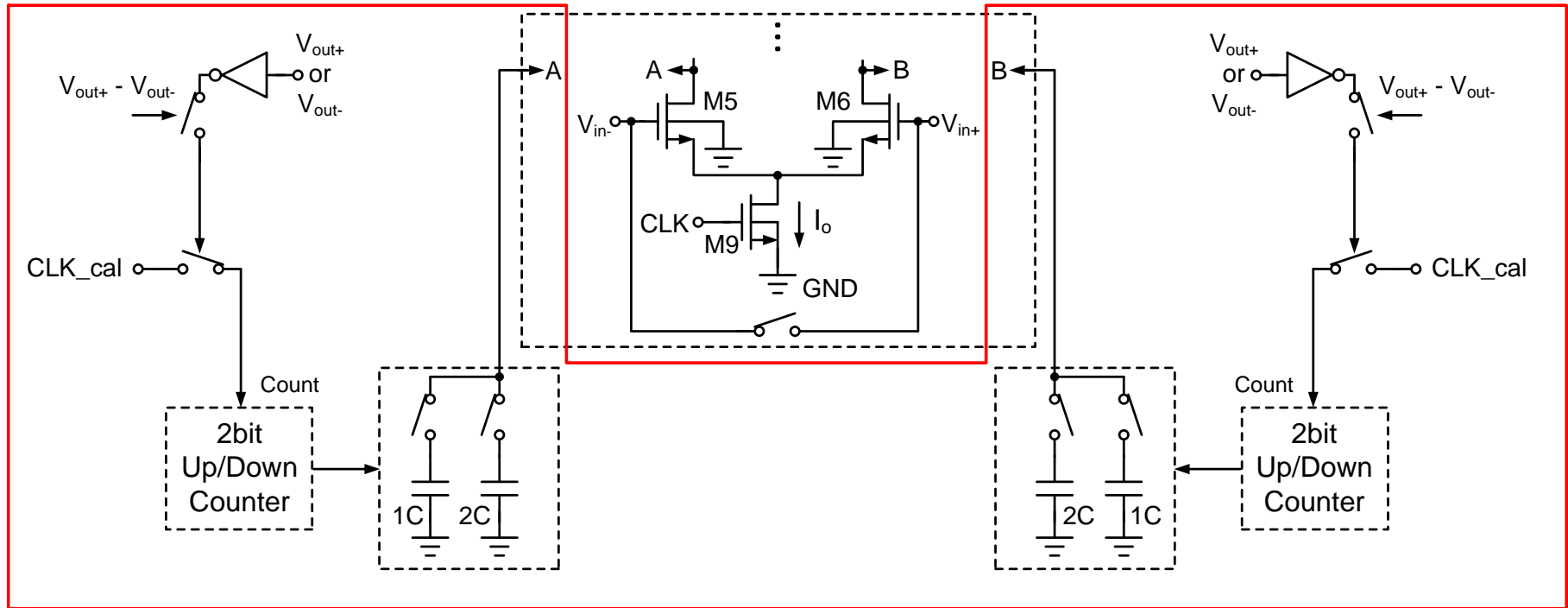
- Circuit diagram



- ◆ CLK off  $\rightarrow$  Reset  $V_{out+}$  and  $V_{out-}$  to  $V_{DD}$
- ◆ CLK on  $\rightarrow \Delta V_{in}$  makes  $I_{M5}$  and  $I_{M6}$  different  
 $\rightarrow$  different discharging speed of  $C_L \rightarrow \Delta V_{out}$   
 $\rightarrow$  latch positive feedback

# Analog IC Design Homework 5 (3/6)

## ● Reference



## ● Note

- ◆ You can design the circuit in red frame by yourself
- ◆ Please finish the offset cancellation before CLK on in P.2. CLK signal in testbench can be modified (But the timing, period,  $t_{on}$  of original turn on state is not changed)
- ◆ Please describe the circuit operation principle in detail

- Reference



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# Analog IC Design Homework 5 (5/6)

- Your report should include
  - ◆ Design flow
  - ◆ HSPICE verification results
    - Please show the waveform and mark the Total compare time, Tc.
  - ◆ Virtuoso schematic (Include the .cir file and circuit diagram)
  - ◆ Area
    - MOSFET : Please calculate the sum of the W\*L for all the MOS used in the designed circuit
$$A_{MOS} = \sum W_i \times L_i$$
    - Capacitor : Just show the capacitance (if used)
    - Resistor : Just show the resistance (if used)
  - ◆ Total current and power consumption (M9 turn on) (including waveform)
  - ◆ Table of specifications

AIC HW5_Name		
Comparator	w/o Offset cancellation circuit	w/ Offset cancellation circuit
Tc (ps)		
Area (μm <sup>2</sup> )		
Current (nA)		

# Analog IC Design Homework 5 (6/6)

## ● Grading

- ◆ Customization of the .sp file will not be accepted
- ◆ Please name all nodes and transistors as shown in P.2 and P.3
- ◆ Under the condition of all circuits are composed of MOS, R and C and meet the test conditions, the smaller Tc, area, and power consumption will receive higher scores. (According to the circuit design of TT corner, please upload the subckt.sp)
- ◆ **Extra points:** Design the offset cancellation circuit in P.3 by yourself.
- ◆ Please **clearly describe the design flow** in your report and attach your **calculation process** (Do not copy)
- ◆ Report with simulation results only but no design flow will get deducted points according to the situation.
- ◆ Report with advanced discussion and analysis will receive higher scores.

## ● Precautions

- ◆ Deadline: [12/07/2025 \(Sun.\) 23:59:59 pm](#) (不接受作業補交)
- ◆ 使用16nm或更先進製程模擬可自定規格，規格愈佳可獲愈高分
- ◆ Personal work, please upload **Word and HSPICE code (.sp file and .cir file)** to moodle
- ◆ Please compress files into a .zip file and name it as HW#\_student ID, ex: HW5\_N26000000 Font size: 12pt (Chinese: 標楷體, English: Times New Roman)
- ◆ Refer to the IEEE submission regulations, set the picture resolution to 300dpi.
- ◆ Upload file size is recommended to be 2MB